HIGH-SPEED 3.3V 8/4K x 18 DUAL-PORT 8/4K x 16 DUAL-PORT STATIC RAM

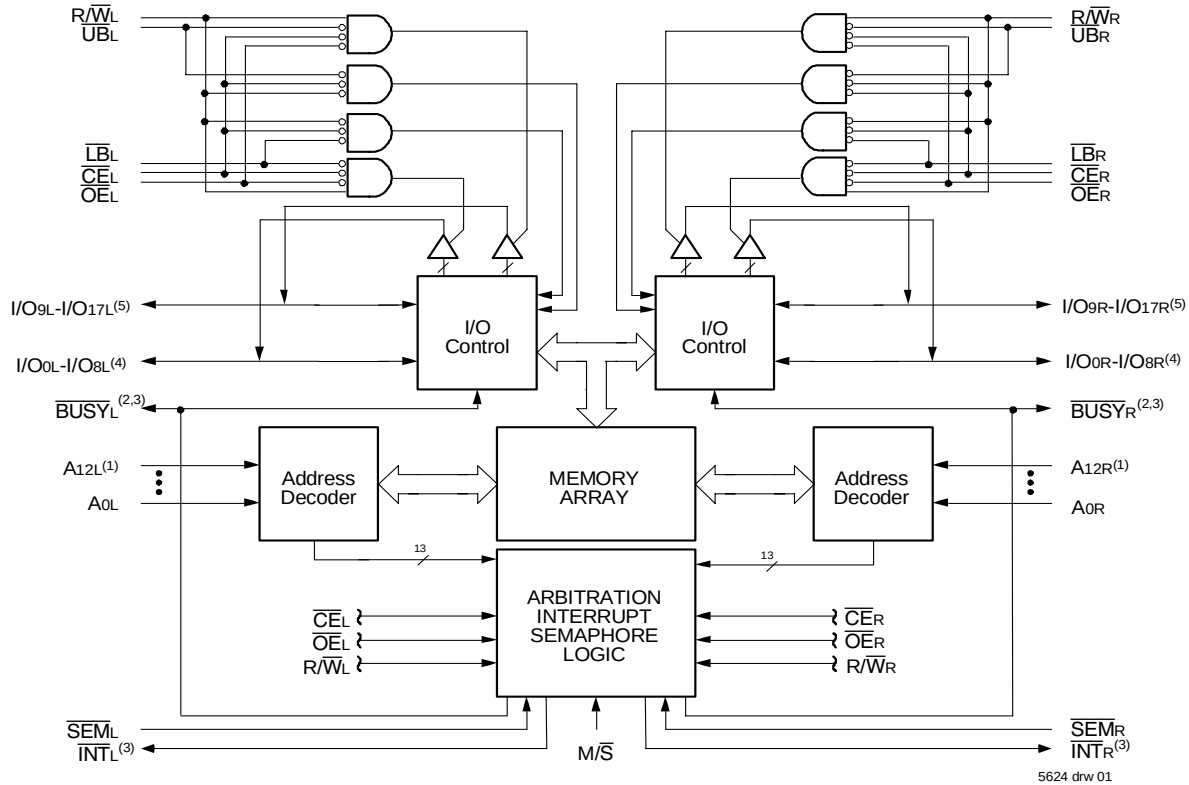
IDT70V35/34S/L
IDT70V25/24S/L

Features

- **True Dual-Ported memory cells which allow simultaneous reads of the same memory location**
- **High-speed access**
  IDT70V35/34
  - *Commercial: 15/20/25ns (max.)*
  - *Industrial: 20ns*

  IDT70V25/24
  - *Commercial: 15/20/25/35/55ns (max.)*
  - *Industrial: 20/25ns*
- **Low-power operation**
  - ***IDT70V35/34S***
    Active: 430mW (typ.)
    Standby: 3.3mW (typ.)
  - ***IDT70V35/34L***
    Active: 415mW (typ.)
    Standby: 660µW (typ.)
  - ***IDT70V25/24S***
    Active: 400mW (typ.)
    Standby: 3.3mW (typ.)
  - ***IDT70V25/24L***
    Active: 380mW (typ.)
    Standby: 660µW (typ.)
- **Separate upper-byte and lower-byte control for multiplexed bus compatibility**
- **IDT70V35/34 (IDT70V25/24) easily expands data bus width to 36 bits (32 bits) or more using the Master/Slave select when cascading more than one device**
- **M/$\overline{S}$ = VIH for $\overline{BUSY}$ output flag on Master**
  M/$\overline{S}$ = VIL for $\overline{BUSY}$ input on Slave
- **$\overline{BUSY}$ and Interrupt Flag**
- **On-chip port arbitration logic**
- **Full on-chip hardware support of semaphore signaling between ports**
- **Fully asynchronous operation from either port**
- **LVTTL-compatible, single 3.3V (±0.3V) power supply**
- **Available in a 100-pin TQFP (IDT70V35/24) & (IDT70V25/24), 86-pin PGA (IDT70V25/24) and 84-pin PLCC (IDT70V25/24)**
- **Industrial temperature range (-40°C to +85°C) is available for selected speeds**
- **Green parts available, see ordering information**

Functional Block Diagram



5624 drw 01

NOTES:
1. A12 is a NC for IDT70V34 and for IDT70V24.
2. (MASTER): $\overline{BUSY}$ is output; (SLAVE): $\overline{BUSY}$ is input.
3. $\overline{BUSY}$ outputs and $\overline{INT}$ outputs are non-tri-stated push-pull.
4. I/O0x - I/O7x for IDT70V25/24.
5. I/O8x - I/O15x for IDT70V25/24.

Description

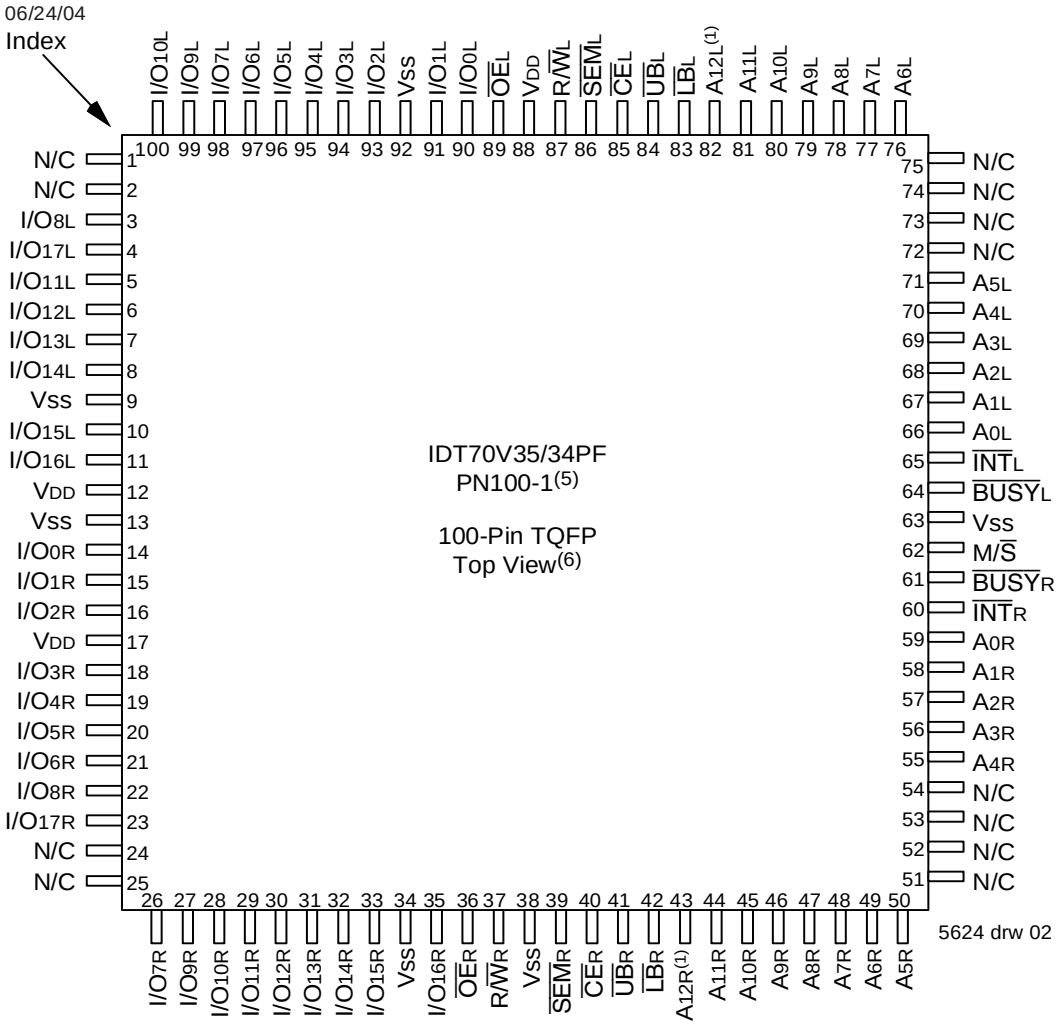
The IDT70V35/34 (IDT70V25/24) is a high-speed 8/4K x 18 (8/4K x16) Dual-Port Static RAM. The IDT70V35/34 (IDT70V25/24) is designed to be used as a stand-alone Dual-Port RAM or as a combination MASTER/SLAVE Dual-Port RAM for 36-bit (32-bit) or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

This device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by $\overline{CE}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 430mW (IDT70V35/34) and 400mW (IDT70V25/24) of power.

The IDT70V35/34 (IDT70V25/24) is packaged in a plastic 100-pin Thin Quad Flatpack. The IDT70V25/24 is packaged in a ceramic 84-pin PGA and 84-Pin PLCC.

Pin Configurations[1,2,3,4]



NOTES:

1. A_{12} is a NC for IDT70V34.
2. All V_{DD} pins must be connected to power supply.
3. All V_{SS} pins must be connected to ground.
4. PN100-1 package body is approximately 14mm x 14mm x 1.4mm.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part marking.

Absolute Maximum Ratings(1)

Symbol	Rating	Commercial & Industrial	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
T_{JN}	Junction Temperature	+150	°C
I_{OUT}	DC Output Current	50	mA

5624 tbl 04

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{DD} + 0.3V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of $V_{TERM} \geq V_{DD}$ + 0.3V.

Capacitance(1) (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	9	pF
C_{OUT}(2)	Output Capacitance	V_{OUT} = 0V	10	pF

5624 tbl 07

NOTES:
1. This parameter is determined by device characterization but is not production tested.
2. C_{OUT} also references $C_{I/O}$.

Maximum Operating Temperature and Supply Voltage(1)

Grade	Ambient Temperature	GND	V_{DD}
Commercial	0°C to +70°C	0V	3.3V ± 0.3V
Industrial	-40°C to +85°C	0V	3.3V ± 0.3V

5624 tbl 05

NOTE:
1. This is the parameter T_A. This is the "instant on" case temperature.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	3.0	3.3	3.6	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	V_{DD}+0.3(2)	V
V_{IL}	Input Low Voltage	-0.3(1)	—	0.8	V

5624 tbl 06

NOTES:
1. $V_{IL} \geq$ -1.5V for pulse width less than 10ns.
2. V_{TERM} must not exceed V_{DD} + 0.3V.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 3.3V ± 0.3V)

Symbol	Parameter	Test Conditions	70V35/34/25/24S		70V35/34/25/24L		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current(1)	V_{DD} = 3.6V, V_{IN} = 0V to V_{DD}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Currentt(1)	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{DD}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = +4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

5624 tbl 08

NOTE:
1. At $V_{DD} \leq$ 2.0V leakages are undefined.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range for 70V25/24[1] (V_{DD} = 3.3V ± 0.3V)

Symbol	Parameter	Test Condition	Version		70V25/24X15 Com'l Only		70V25/24X20 Com'l & Ind		70V25/24X25 Com'l & Ind		Unit
					Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.	
I_{DD}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open $\overline{SEM}$ = V_{IH} f = f_{MAX}[3]	COM'L	S	150	215	140	200	130	190	mA
				L	140	185	130	175	125	165	
			IND	S	—	—	140	225	—	—	
				L	—	—	130	195	125	180	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_R$ and $\overline{CE}_L$ = V_{IH} $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH} f = f_{MAX}[3]	COM'L	S	25	35	20	30	16	30	mA
				L	20	30	15	25	13	25	
			MIL & IND	S	—	—	20	45	—	—	
				L	—	—	15	40	13	40	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_{"A"}$ = V_{IL} and $\overline{CE}_{"B"}$ = V_{IH}[5] Active Port Outputs Open, f=f_{MAX}[3] $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH}	COM'L	S	85	120	80	110	75	110	mA
				L	80	110	75	100	72	95	
			MIL & IND	S	—	—	80	130	—	—	
				L	—	—	75	115	72	110	
I_{SB3}	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{DD} - 0.2V, V_{IN} ≥ V_{DD} - 0.2V or V_{IN} ≤ 0.2V, f = 0[4] $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ V_{DD} - 0.2V	COM'L	S	1.0	5	1.0	5	1.0	5	mA
				L	0.2	2.5	0.2	2.5	0.2	2.5	
			MIL & IND	S	—	—	1.0	15	—	—	
				L	—	—	0.2	5	0.2	5	
I_{SB4}	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}_{"A"}$ ≤ 0.2V and $\overline{CE}_{"B"}$ ≥ V_{DD} - 0.2V[5] $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ V_{DD} - 0.2V V_{IN} ≥ V_{DD} - 0.2V or V_{IN} ≤ 0.2V Active Port Outputs Open, f = f_{MAX}[3]	COM'L	S	85	125	80	115	75	105	mA
				L	80	105	75	100	70	90	
			MIL & IND	S	—	—	80	130	—	—	
				L	—	—	75	115	70	105	

5624 tbl 09a

Symbol	Parameter	Test Condition	Version		70V25/24X35 Com'l Only		70V25/24X55 Com'l Only		Unit
					Typ.[2]	Max.	Typ.[2]	Max.	
I_{DD}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open $\overline{SEM}$ = V_{IH} f = f_{MAX}[3]	COM'L	S	120	180	120	180	mA
				L	115	155	115	155	
			IND	S	—	—	—	—	
				L	—	—	—	—	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_R$ and $\overline{CE}_L$ = V_{IH} $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH} f = f_{MAX}[3]	COM'L	S	13	25	13	25	mA
				L	11	20	11	20	
			MIL & IND	S	—	—	—	—	
				L	—	—	—	—	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_{"A"}$ = V_{IL} and $\overline{CE}_{"B"}$ = V_{IH}[5] Active Port Outputs Open, f=f_{MAX}[3] $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH}	COM'L	S	70	100	70	100	mA
				L	65	90	65	90	
			MIL & IND	S	—	—	—	—	
				L	—	—	—	—	
I_{SB3}	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{DD} - 0.2V, V_{IN} ≥ V_{DD} - 0.2V or V_{IN} ≤ 0.2V, f = 0[4] $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ V_{DD} - 0.2V	COM'L	S	1.0	5	1.0	5	mA
				L	0.2	2.5	0.2	2.5	
			MIL & IND	S	—	—	—	—	
				L	—	—	—	—	
I_{SB4}	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}_{"A"}$ ≤ 0.2V and $\overline{CE}_{"B"}$ ≥ V_{DD}- 0.2V[5] $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ V_{DD} - 0.2V V_{IN} ≥ V_{DD} - 0.2V or V_{IN} ≤ 0.2V Active Port Outputs Open, f = f_{MAX}[3]	COM'L	S	65	100	65	100	mA
				L	60	85	60	85	
			MIL & IND	S	—	—	—	—	
				L	—	—	—	—	

5624 tbl 09b

NOTES:

1. 'X' in part number indicates power rating (S or L)
2. V_{DD} = 3.3V, T_A = +25°C, and are not production tested. $I_{DD\,DC}$ = 115mA (typ.)
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.
5. Port "A" may be either left or right port. Port "B" is the opposite from port "A".

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range for 70V25/24[4]

Symbol	Parameter	70V25/24X15 Com'l Only		70V25/24X20 Com'l & Ind		70V25/24X25 Com'l & Ind		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	15	—	20	—	25	—	ns
t_{AA}	Address Access Time	—	15	—	20	—	25	ns
t_{ACE}	Chip Enable Access Time[3]	—	15	—	20	—	25	ns
t_{ABE}	Byte Enable Access Time[3]	—	15	—	20	—	25	ns
t_{AOE}	Output Enable Access Time[3]	—	10	—	12	—	13	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
t_{LZ}	Output Low-Z Time[1,2]	3	—	3	—	3	—	ns
t_{HZ}	Output High-Z Time[1,2]	—	10	—	12	—	15	ns
t_{PU}	Chip Enable to Power Up Time[1,2]	0	—	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time[1,2]	—	15	—	20	—	25	ns
t_{SOP}	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10	—	10	—	10	—	ns
t_{SAA}	Semaphore Address Access[3]	—	15	—	20	—	25	ns

5624 tbl 11a

Symbol	Parameter	70V25/24X35 Com'l Only		70V25/24X55 Com'l Only		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t_{RC}	Read Cycle Time	35	—	55	—	ns
t_{AA}	Address Access Time	—	35	—	55	ns
t_{ACE}	Chip Enable Access Time[3]	—	35	—	55	ns
t_{ABE}	Byte Enable Access Time[3]	—	35	—	55	ns
t_{AOE}	Output Enable Access Time[3]	—	20	—	30	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	ns
t_{LZ}	Output Low-Z Time[1,2]	3	—	3	—	ns
t_{HZ}	Output High-Z Time[1,2]	—	15	—	25	ns
t_{PU}	Chip Enable to Power Up Time[1,2]	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time[1,2]	—	35	—	50	ns
t_{SOP}	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	15	—	ns
t_{SAA}	Semaphore Address Access[3]	—	35	—	55	ns

5624 tbl 11b

NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access RAM, $\overline{CE}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_{IL}, and $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CE}$ = V_{IH} or $\overline{UB}$ & $\overline{LB}$ = V_{IH}, and $\overline{SEM}$ = V_{IL}.
4. 'X' in part number indicates power rating (S or L).

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage for 70V25/24 (5)

Symbol	Parameter	70V25/24X15 Com'l Only		70V25/24X20 Com'l & Ind		70V25/24X25 Com'l & Ind		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
t_{WC}	Write Cycle Time	15	—	20	—	25	—	ns
t_{EW}	Chip Enable to End-of-Write(3)	12	—	15	—	20	—	ns
t_{AW}	Address Valid to End-of-Write	12	—	15	—	20	—	ns
t_{AS}	Address Set-up Time(3)	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	12	—	15	—	20	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	10	—	15	—	15	—	ns
t_{HZ}	Output High-Z Time(1,2)	—	10	—	12	—	15	ns
t_{DH}	Data Hold Time(4)	0	—	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High-Z(1,2)	—	10	—	12	—	15	ns
t_{OW}	Output Active from End-of-Write(1,2,4)	0	—	0	—	0	—	ns
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	5	—	5	—	5	—	ns
t_{SPS}	$\overline{SEM}$ Flag Contention Window	5	—	5	—	5	—	ns

5624 tbl 12a

Symbol	Parameter	70V25/24X35 Com'l Only		70V25/24X55 Com'l Only		Unit
		Min.	Max.	Min.	Max.	
WRITE CYCLE						
t_{WC}	Write Cycle Time	35	—	55	—	ns
t_{EW}	Chip Enable to End-of-Write(3)	30	—	45	—	ns
t_{AW}	Address Valid to End-of-Write	30	—	45	—	ns
t_{AS}	Address Set-up Time(3)	0	—	0	—	ns
t_{WP}	Write Pulse Width	25	—	40	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	15	—	30	—	ns
t_{HZ}	Output High-Z Time(1,2)	—	15	—	25	ns
t_{DH}	Data Hold Time(4)	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High-Z(1,2)	—	15	—	25	ns
t_{OW}	Output Active from End-of-Write(1,2,4)	0	—	0	—	ns
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	5	—	5	—	ns
t_{SPS}	$\overline{SEM}$ Flag Contention Window	5	—	5	—	ns

5624 tbl 12b

NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access SRAM, $\overline{CE}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_{IL}, $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CE}$ = V_{IH} or $\overline{UB}$ & $\overline{LB}$ = V_{IH}, and $\overline{SEM}$ = V_{IL}. Either condition must be valid for the entire t_{EW} time.
4. The specification for t_{DH} must be met by the device supplying write data to the SRAM under all operating conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.
5. 'X' in part number indicates power rating (S or L).

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range for 70V25/24[6]

Symbol	Parameter	70V25/24X15 Com'l Ony		70V25/24X20 Com'l & Ind		70V25/24X25 Com'l & Ind		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
$\overline{BUSY}$ TIMING (M/$\overline{S}$ = V_{IH})								
t_{BAA}	$\overline{BUSY}$ Access Time from Address Match	—	15	—	20	—	20	ns
t_{BDA}	$\overline{BUSY}$ Disable Time from Address Not Matched	—	15	—	20	—	20	ns
t_{BAC}	$\overline{BUSY}$ Access Time from Chip Enable LOW	—	15	—	20	—	20	ns
t_{BDC}	$\overline{BUSY}$ Disable Time from Chip Enable HIGH	—	15	—	17	—	17	ns
t_{APS}	Arbitration Priority Set-up Time[2]	5	—	5	—	5	—	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Data[3]	—	18	—	30	—	30	ns
t_{WH}	Write Hold After $\overline{BUSY}$[5]	12	—	15	—	17	—	ns
$\overline{BUSY}$ TIMING (M/$\overline{S}$ = V_{IL})								
t_{WB}	$\overline{BUSY}$ Input to Write[4]	0	—	0	—	0	—	ns
t_{WH}	Write Hold After $\overline{BUSY}$[5]	12	—	15	—	17	—	ns
PORT-TO-PORT DELAY TIMING								
t_{WDD}	Write Pulse to Data Delay[1]	—	30	—	45	—	50	ns
t_{DDD}	Write Data Valid to Read Data Delay[1]	—	25	—	35	—	35	ns

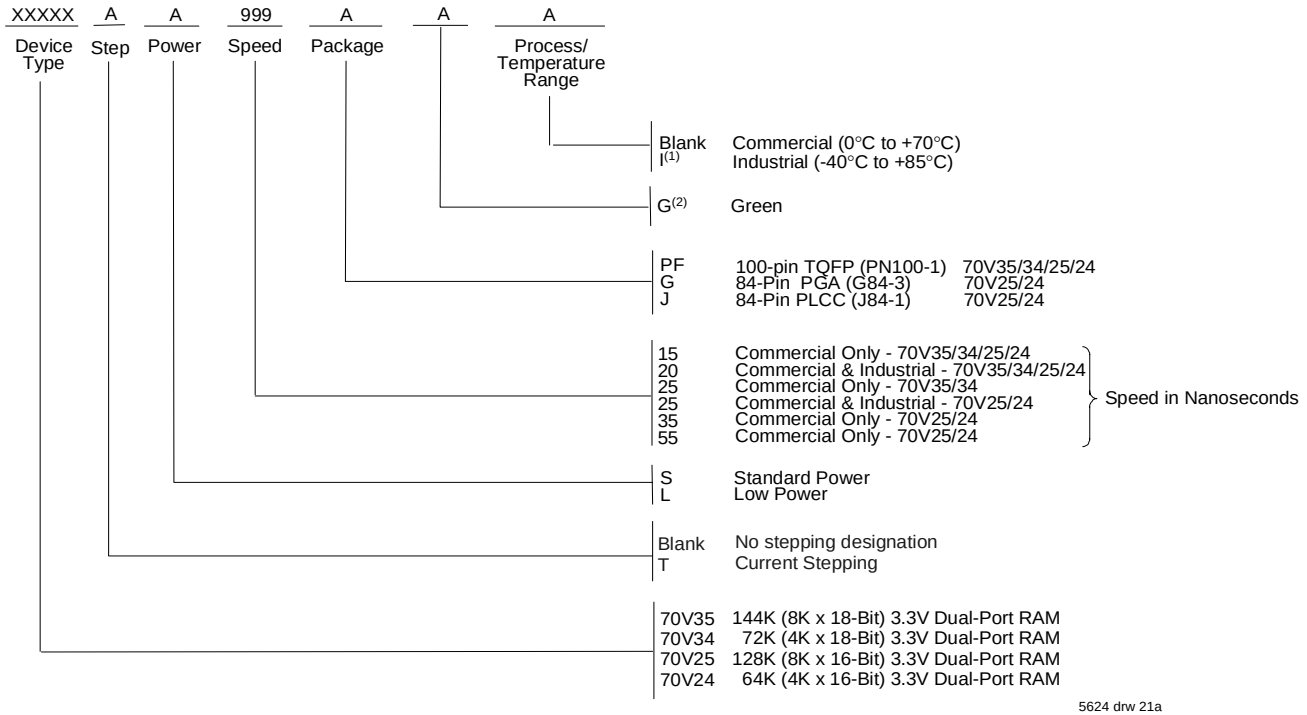
5624 tbl 13a

Symbol	Parameter	70V25/24X35 Com'l Only		70V25/24X55 Com'l Only		Unit
		Min.	Max.	Min.	Max.	
$\overline{BUSY}$ TIMING (M/$\overline{S}$ = V_{IH})						
t_{BAA}	$\overline{BUSY}$ Access Time from Address Match	—	20	—	45	ns
t_{BDA}	$\overline{BUSY}$ Disable Time from Address Not Matched	—	20	—	40	ns
t_{BAC}	$\overline{BUSY}$ Access Time from Chip Enable LOW	—	20	—	40	ns
t_{BDC}	$\overline{BUSY}$ Disable Time from Chip Enable HIGH	—	20	—	35	ns
t_{APS}	Arbitration Priority Set-up Time[2]	5	—	5	—	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Data[3]	—	35	—	40	ns
t_{WH}	Write Hold After $\overline{BUSY}$[5]	25	—	25	—	ns
$\overline{BUSY}$ TIMING (M/$\overline{S}$ = V_{IL})						
t_{WB}	$\overline{BUSY}$ Input to Write[4]	0	—	0	—	ns
t_{WH}	Write Hold After $\overline{BUSY}$[5]	25	—	25	—	ns
PORT-TO-PORT DELAY TIMING						
t_{WDD}	Write Pulse to Data Delay[1]	—	60	—	80	ns
t_{DDD}	Write Data Valid to Read Data Delay[1]	—	45	—	65	ns

5624 tbl 13b

NOTES:
1. Port-to-port delay through SRAM cells from writing port to reading port, refer to "TIMING WAVEFORM OF WRITE PORT-TO-PORT READ AND $\overline{BUSY}$ (M/$\overline{S}$ = V_{IH})".
2. To ensure that the earlier of the two ports wins.
3. t_{BDD} is a calculated parameter and is the greater of 0, $t_{WDD} - t_{WP}$ (actual) or $t_{DDD} - t_{DW}$ (actual).
4. To ensure that the write cycle is inhibited during contention.
5. To ensure that a write cycle is completed after contention.
6. 'X' in part number indicates power rating (S or L).

Ordering Information



5624 drw 21a

NOTES:

1. Contact your local sales office for Industrial temp range for other speeds, packages and powers.
2. Green parts available. For specific speeds, packages and powers contact your local sales office.